# EAST Search History

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 12 | ("6720673" "6711719" "6825711" "6574779" "6667648" "6820240").pn. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 10:05 |
| L2 | 2 | ("6667648").URPN. | USPAT | OR | ON | 2006/06/17 10:10 |
| L3 | 12 | ("5374861" \| "5608757" \| "5699002" \| "5737364" \| "5748024" \| "5796299" \| "5917358" \| "6208494" \| "6362644" \| "6433585" \| "6472911" \| "6545521").PN. | US-PGPUB; USPAT; USOCR | OR | ON | 2006/06/17 10:16 |
| L4 | 1 | ((slecti$4 or adapt$5)near3 ((disabl$4 or remov$4 or de$power$4)near2 (power or voltage or supply)))with ((processing or input or output) adj3 island$1) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 10:31 |
| L5 | 1 | ((slecti$4 or adapt$5)near3 ((disabl$4 or remov$4 or de$power$4)near2 (power or voltage or supply)))same ((processing or input or output) adj3 island$1) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 10:32 |
| L6 | 1 | ( ((disabl$4 or remov$4 or de$power$4)near2 (power or voltage or supply)))same ((processing or input or output) adj3 island$1) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 10:33 |
| L7 | 1 | (( ((disabl$4 or remov$4 or de$power$4)near2 (power or voltage or supply)))same ((processing or input or output) adj3 island$1)).clm. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 10:33 |
| L8 | 1 | ( ((disabl$4 or remov$4 or de$power$4 or disconnect$4 or deactivat$4)near2 (power or voltage or supply)))same ((processing or input or output) adj3 island$1) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 10:33 |

# EAST Search History

| | | | | | | |
|---|---|---|---|---|---|---|
| L9 | 1 | ( ((disabl$4 or remov$4 or de$power$4 or disconnect$4 or deactivat$4 or suspend$4)near2 (power or voltage or supply)))same ((processing or input or output) adj3 island$1) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 11:03 |
| L10 | 283 | ( ((disabl$4 or remov$4 or de$power$4 or disconnect$4 or deactivat$4 or suspend$4)near2 (power or voltage or supply)))with ((processing or input or output) adj3 (partition$4 or part or section or zone or region or island$1)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 10:36 |
| L11 | 4 | l10 same ((semiconductor or integrated)adj circuit) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 12:29 |
| L12 | 53 | l10 and ((semiconductor or integrated)adj circuit) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 10:46 |
| L13 | 11343 | ((semiconductor or integrated)adj circuit)and ((processing or input or output)adj (island$1 or section$1 or region$1 or zon$2 or area$1)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 10:47 |
| L14 | 930 | ((semiconductor or integrated)adj circuit)with ((processing or input or output)adj (island$1 or section$1 or region$1 or zon$2 or area$1)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 10:47 |
| L15 | 3 | l14 same ((power or supply or voltage)near4 (disabl$4 or remov$3 or inactivat$4 or disconnect$4 or deactivat$4)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 10:49 |
| L16 | 59 | l14 and ((power or supply or voltage)near4 (disabl$4 or remov$3 or inactivat$4 or disconnect$4 or deactivat$4)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 10:50 |

# EAST Search History

| | | | | | | |
|---|---|---|---|---|---|---|
| L17 | 1 | l14 and (((power or supply or voltage)near4 (disabl$4 or remov$3 or inactivat$4 or disconnect$4 or deactivat$4))with (trnamission or transfer )) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 10:52 |
| L18 | 7 | l14 and (((power or supply or voltage)near4 (disabl$4 or remov$3 or inactivat$4 or disconnect$4 or deactivat$4))same (tranmission or transfer )) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 12:28 |
| L19 | 0 | ("6950044").URPN. | USPAT | OR | ON | 2006/06/17 11:00 |
| L20 | 8 | ("5422807" \| "5576708" \| "5617090" \| "5920275" \| "6094154" \| "6369738" \| "6556164" \| "6703961").PN. | US-PGPUB; USPAT; USOCR | OR | ON | 2006/06/17 11:02 |
| L21 | 25737 | "713"/$.ccls. | US-PGPUB; USPAT; USOCR | OR | ON | 2006/06/17 11:02 |
| L22 | 90192 | "327"/$.ccls. | US-PGPUB; USPAT; USOCR | OR | ON | 2006/06/17 11:02 |
| L23 | 112977 | "438"/$.ccls. | US-PGPUB; USPAT; USOCR | OR | ON | 2006/06/17 11:03 |
| L24 | 10221 | "716"/$.ccls. | US-PGPUB; USPAT; USOCR | OR | ON | 2006/06/17 11:03 |
| L25 | 50096 | "307"/$.ccls. | US-PGPUB; USPAT; USOCR | OR | ON | 2006/06/17 11:03 |
| L26 | 0 | l21 and (( ((disabl$4 or remov$4 or de$power$4 or disconnect$4 or deactivat$4 or suspend$4)near2 (power or voltage or supply)))same ((processing or input or output) adj3 island$1)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 11:04 |
| L27 | 0 | l22 and (( ((disabl$4 or remov$4 or de$power$4 or disconnect$4 or deactivat$4 or suspend$4)near2 (power or voltage or supply)))same ((processing or input or output) adj3 island$1)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 11:04 |

# EAST Search History

| | | | | | | |
|---|---|---|---|---|---|---|
| L28 | 0 | l23 and (( ((disabl$4 or remov$4 or de$power$4 or disconnect$4 or deactivat$4 or suspend$4)near2 (power or voltage or supply)))same ((processing or input or output) adj3 island$1)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 11:04 |
| L29 | 0 | l24 and (( ((disabl$4 or remov$4 or de$power$4 or disconnect$4 or deactivat$4 or suspend$4)near2 (power or voltage or supply)))same ((processing or input or output) adj3 island$1)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 11:04 |
| L30 | 0 | l25 and (( ((disabl$4 or remov$4 or de$power$4 or disconnect$4 or deactivat$4 or suspend$4)near2 (power or voltage or supply)))same ((processing or input or output) adj3 island$1)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 12:07 |
| L31 | 0 | (((first or one) adj circuit)with ((second or other) adj circuit))with (indpependent adj2 (voltage or power or supply)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 12:10 |
| L32 | 23 | (((first or one) adj circuit)with ((second or other) adj circuit))with (independent adj2 (voltage or power or supply)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 12:10 |
| L33 | 113 | l21 and (((power or supply or voltage)near4 (disabl$4 or remov$3 or inactivat$4 or disconnect$4 or deactivat$4))same (tranmission or transfer )) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 12:28 |
| L34 | 302 | l22 and (((power or supply or voltage)near4 (disabl$4 or remov$3 or inactivat$4 or disconnect$4 or deactivat$4))same (tranmission or transfer )) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 12:28 |
| L35 | 135 | l23 and (((power or supply or voltage)near4 (disabl$4 or remov$3 or inactivat$4 or disconnect$4 or deactivat$4))same (tranmission or transfer )) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 12:28 |

# EAST Search History

| | | | | | | |
|---|---|---|---|---|---|---|
| L36 | 10 | l24 and (((power or supply or voltage)near4 (disabl$4 or remov$3 or inactivat$4 or disconnect$4 or deactivat$4))same (tranmission or transfer )) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 12:30 |
| L37 | 404 | l25 and (((power or supply or voltage)near4 (disabl$4 or remov$3 or inactivat$4 or disconnect$4 or deactivat$4))same (tranmission or transfer )) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 12:28 |
| L38 | 49 | l33 and ((semiconductor or integrated)adj circuit) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 13:42 |
| L39 | 105 | l34 and ((semiconductor or integrated)adj circuit) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 12:29 |
| L40 | 55 | l35 and ((semiconductor or integrated)adj circuit) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 13:30 |
| L41 | 7 | l36 and ((semiconductor or integrated)adj circuit) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 13:50 |
| L42 | 2 | ("6667648").URPN. | USPAT | OR | ON | 2006/06/17 12:53 |
| L43 | 6 | ("6462976" \| "6598148" \| "6631502" \| "6667648" \| "6779163" \| "6820240").PN. | US-PGPUB; USPAT; USOCR | OR | ON | 2006/06/17 13:09 |
| L44 | 2 | ("6137188" "6577535").PN. | US-PGPUB; USPAT; USOCR | OR | ON | 2006/06/17 13:09 |
| L45 | 1 | ("6577535").URPN. | USPAT | OR | ON | 2006/06/17 13:13 |

# EAST Search History

| | | | | | | |
|---|---|---|---|---|---|---|
| L46 | 34 | ("4433282" \| "4578772" \| "4970692" \| "5172338" \| "5196739" \| "5267218" \| "5276646" \| "5291446" \| "5305275" \| "5306961" \| "5388084" \| "5394027" \| "5418752" \| "5426391" \| "5430859" \| "5440520" \| "5442586" \| "5444664" \| "5455794" \| "5508971" \| "5511026" \| "5519654" \| "5524231" \| "5553261" \| "5563825" \| "5568424" \| "5592420" \| "5596532" \| "5598370" \| "5621685" \| "5671179" \| "5693570" \| "5694360" \| "5818781").PN. | US-PGPUB; USPAT; USOCR | OR | ON | 2006/06/17 13:14 |
| L47 | 0 | (JP2002-207528 JP6-255213 JP5-32018 JP5-273950 JP9-247543 JP9-63188 CN1262466A).pn. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 13:43 |
| L48 | 0 | (JP2002207528 JP6255213 JP532018 JP5273950 JP9247543 JP963188 CN1262466A).pn. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 13:44 |
| L49 | 2 | ("2002207528" JP6255213 JP532018 JP5273950 JP9247543 JP963188 CN1262466A).pn. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 13:44 |
| L50 | 14 | ("2002207528" "6255213" "532018" "5273950" "9247543" "963188" 1262466A).pn. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 13:44 |
| L51 | 49 | l33 and ((semiconductor or integrated)adj circuit) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 13:50 |

# EAST Search History

| | | | | | | |
|---|---|---|---|---|---|---|
| L52 | 105 | l34 and ((semiconductor or integrated)adj circuit) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 13:55 |
| L53 | 0 | l52 and island$1 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 13:58 |
| L54 | 896 | ((power or voltage or current)near5 (control$4 or manag$5 or reduc$5 or sav$4 or disabl$4 or inactivat$4)) with island$1 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 14:00 |
| L55 | 0 | ((power or voltage or current)near5 (control$4 or manag$5 or reduc$5 or sav$4 or disabl$4 or inactivat$4 or remov$4 or disconnect$4)) with island$1 with ((transfer or transmi$4 or transmission) adj complet$4) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 14:02 |
| L56 | 0 | ((power or voltage or current)near5 (control$4 or manag$5 or reduc$5 or sav$4 or disabl$4 or inactivat$4 or remov$4 or disconnect$4)) with island$1 same ((transfer or transmi$4 or transmission) adj complet$4) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 14:02 |
| L57 | 0 | ((power or voltage or current)near5 (control$4 or manag$5 or reduc$5 or sav$4 or disabl$4 or inactivat$4 or remov$4 or disconnect$4)) with island$1 same ((transfer or transmi$4 or transmission) adj (finish$4 or complet$4 or done)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 14:04 |
| L58 | 3 | ((power or voltage or current)near5 (control$4 or manag$5 or reduc$5 or sav$4 or disabl$4 or inactivat$4 or remov$4 or disconnect$4)) same island$1 same ((transfer or transmi$4 or transmission) adj (finish$4 or complet$4 or done)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 14:09 |

# EAST Search History

| | | | | | | |
|---|---|---|---|---|---|---|
| L59 | 25 | ((semiconductor or integrated)adj2 (circuit or IC))same (process$4 adj (isalnd or section or block or circuit or zone))same (input adj (isalnd or section or block or circuit or zone))same (output adj (isalnd or section or block or circuit or zone)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 14:35 |
| L60 | 0 | l59 and (((power or voltage or current)near5 (control$4 or manag$5 or reduc$5 or sav$4 or disabl$4 or inactivat$4 or remov$4 or disconnect$4))same ((transfer or transmi$4 or transmission) adj (finish$4 or complet$4 or done))) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 14:10 |
| L61 | 1 | l59 and (((power or voltage or current)near5 (control$4 or manag$5 or reduc$5 or sav$4 or disabl$4 or inactivat$4 or remov$4 or disconnect$4))same ( (finish$4 or complet$4 or done))) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 14:10 |
| L62 | 2 | ("6820240").pn. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 14:29 |
| L63 | 71 | ((power or voltage or supply or current)near3 (remov$4 or disabl$4 or disconnect$4 or inactivat$4))with (transmission near3 (complet$4 or done or finish$3)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 14:31 |
| L64 | 0 | l63 and (((semiconductor or integrated)adj2 (circuit or IC))same (process$4 adj (isalnd or section or block or circuit or zone))same (input adj (isalnd or section or block or circuit or zone))same (output adj (isalnd or section or block or circuit or zone))) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/17 14:36 |

PALM INTRANET

Day : Saturday
Date: 6/17/2006
Time: 09:55:45

## Inventor Name Search Result

Your Search was:

Last Name = BLANCO
First Name = RAFAEL

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|---|---|---|---|---|---|
| 08224927 | 5554946 | 150 | 04/08/1994 | TIMING SIGNAL GENERATOR | BLANCO, RAFAEL |
| 08453587 | 5568075 | 150 | 05/30/1995 | TIMING SIGNAL GENERATOR | BLANCO, RAFAEL |
| 09832520 | 6720673 | 150 | 04/11/2001 | VOLTAGE ISLAND FENCING | BLANCO, RAFAEL |
| 10604328 | Not Issued | 30 | 07/11/2003 | POWER DOWN PROCESSING ISLANDS | BLANCO, RAFAEL |
| 10904056 | Not Issued | 30 | 10/21/2004 | SIMULATION TESTING OF DIGITAL LOGIC CIRCUIT DESIGNS | BLANCO, RAFAEL |
| 10906476 | Not Issued | 30 | 02/22/2005 | METHOD OF SWITCHING VOLTAGE ISLANDS IN INTEGRATED CIRCUITS | BLANCO, RAFAEL |
| 11160184 | Not Issued | 30 | 08/19/2005 | SELECTIVELY CHANGEABLE LINE WIDTH MEMORY | BLANCO, RAFAEL |

Inventor Search Completed: No Records to Display.

**Search Another: Inventor**

**Last Name** BLANCO **First Name** RAFAEL Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

PALM INTRANET

Day : Saturday
Date: 6/17/2006
Time: 09:56:36

## Inventor Name Search Result

Your Search was:

Last Name = COHN
First Name = JOHN

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|---|---|---|---|---|---|
| 09057961 | 6189132 | 150 | 04/09/1998 | DESIGN RULE CORRECTION SYSTEM AND METHOD | COHN, JOHN |
| 11382601 | Not Issued | 20 | 05/10/2006 | UTILIZING CLOCK SHIELD AS DEFECT MONITOR | COHN, JOHN M |
| 09616485 | Not Issued | 168 | 07/14/2000 | Low input impedance line/bus receiver | COHN, JOHN M. |
| 09702313 | 6473881 | 150 | 10/31/2000 | PATTERN-MATCHING FOR TRANSISTOR LEVEL NETLISTS | COHN, JOHN M. |
| 09705031 | 6429469 | 150 | 11/02/2000 | OPTICAL PROXIMITY CORRECTION STRUCTURES HAVING DECOUPLING CAPACITORS | COHN, JOHN M. |
| 09713829 | 6792582 | 150 | 11/15/2000 | CONCURRENT LOGICAL AND PHYSICAL CONSTRUCTION OF VOLTAGE ISLANDS FOR MIXED SUPPLY VOLTAGE DESIGNS | COHN, JOHN M. |
| 09737012 | 6523154 | 150 | 12/14/2000 | METHOD FOR SUPPLY VOLTAGE DROP ANALYSIS DURING PLACEMENT PHASE OF CHIP DESIGN | COHN, JOHN M. |
| 09750969 | 6687883 | 150 | 12/28/2000 | SYSTEM AND METHOD FOR INSERTING LEAKAGE REDUCTION CONTROL IN LOGIC CIRCUITS | COHN, JOHN M. |
| 09761464 | 6523159 | 150 | 01/16/2001 | METHOD FOR ADDING DECOUPLING CAPACITANCE DURING INTEGRATED CIRCUIT DESIGN | COHN, JOHN M. |
| 09781369 | 6985004 | 150 | 02/12/2001 | WIRING OPTIMIZATIONS FOR POWER | COHN, JOHN M. |
| 09812211 | 6490708 | 150 | 03/19/2001 | METHOD OF INTEGRATED CIRCUIT DESIGN BY SELECTION OF NOISE TOLERANT GATES | COHN, JOHN M. |
| 09833479 | 6574779 | 150 | 04/12/2001 | HIERARCHICAL LAYOUT METHOD FOR INTEGRATED CIRCUITS | COHN, JOHN M. |
| 10248324 | 6948146 | 150 | 01/09/2003 | SIMPLIFIED TILING PATTERN METHOD | COHN, JOHN M. |
| 10248696 | 6924661 | 150 | 02/10/2003 | POWER SWITCH CIRCUIT SIZING TECHNIQUE | COHN, JOHN M. |

| | | | | | |
|---|---|---|---|---|---|
| 10249684 | 6825711 | 150 | 04/30/2003 | POWER REDUCTION BY STAGE IN INTEGRATED CIRCUIT | COHN, JOHN M. |
| 10249779 | Not Issued | 95 | 05/07/2003 | MULTIPLE SUPPLY GATE ARRAY BACKFILL STRUCTURE | COHN, JOHN M. |
| 10250295 | Not Issued | 30 | 06/20/2003 | METHOD AND APPARATUS FOR MANUFACTURING DIAMOND SHAPED CHIPS | COHN, JOHN M. |
| 10604328 | Not Issued | 30 | 07/11/2003 | POWER DOWN PROCESSING ISLANDS | COHN, JOHN M. |
| 10709672 | Not Issued | 30 | 05/21/2004 | LEARNING BASED LOGIC DIAGNOSIS | COHN, JOHN M. |
| 10709754 | Not Issued | 30 | 05/26/2004 | A SYSTEM AND METHOD OF PROVIDING ERROR DETECTION AND CORRECTION CAPABILITY IN AN INTEGRATED CIRCUIT USING REDUNDANT LOGIC CELLS OF AN EMBEDDED FPGA | COHN, JOHN M. |
| 10710114 | Not Issued | 95 | 06/18/2004 | METHOD AND STRUCTURE FOR DEFECT MONITORING OF SEMICONDUCTOR DEVICES USING POWER BUS WIRING GRIDS | COHN, JOHN M. |
| 10710222 | 7005874 | 150 | 06/28/2004 | UTILIZING CLOCK SHIELD AS DEFECT MONITOR | COHN, JOHN M. |
| 10710640 | 6998866 | 150 | 07/27/2004 | CIRCUIT AND METHOD FOR MONITORING DEFECTS | COHN, JOHN M. |
| 10710642 | Not Issued | 30 | 07/27/2004 | Designing Scan Chains With Specific Parameter Sensitivities to Identify Process Defects | COHN, JOHN M. |
| 10710879 | Not Issued | 94 | 08/10/2004 | DEFECT DIAGNOSIS FOR SEMICONDUCTOR INTEGRATED CIRCUITS | COHN, JOHN M. |
| 10710940 | Not Issued | 93 | 08/13/2004 | METHOD FOR DESIGNING AN INTEGRATED CIRCUIT DEFECT MONITOR | COHN, JOHN M. |
| 10906476 | Not Issued | 30 | 02/22/2005 | METHOD OF SWITCHING VOLTAGE ISLANDS IN INTEGRATED CIRCUITS | COHN, JOHN M. |
| 10906591 | Not Issued | 30 | 02/25/2005 | CIRCUIT LAYOUT METHODOLOGY | COHN, JOHN M. |
| 10907494 | Not Issued | 30 | 04/04/2005 | METHOD OF ADDING FABRICATION MONITORS TO INTEGRATED CIRCUIT CHIPS | COHN, JOHN M. |
| 10908593 | Not Issued | 30 | 05/18/2005 | THE USE OF REDUNDANT ROUTES TO INCREASE THE YIELD AND RELIABILITY OF A VLSI LAYOUT | COHN, JOHN M. |
| 10917193 | Not Issued | 30 | 08/12/2004 | Physical design system and method | COHN, JOHN M. |
| 11160266 | Not | 25 | 06/16/2005 | INTEGRATED CIRCUIT DIAGNOSING | COHN, JOHN M. |

| | | | | | |
|---|---|---|---|---|---|
| | Issued | | | METHOD, SYSTEM, AND PROGRAM PRODUCT | |
| 11160339 | Not Issued | 30 | 06/20/2005 | IC TILING PATTERN METHOD, IC SO FORMED AND ANALYSIS METHOD | COHN, JOHN M. |
| 11176712 | Not Issued | 25 | 07/07/2005 | Wiring optimizations for power | COHN, JOHN M. |
| 11275076 | Not Issued | 25 | 12/08/2005 | A METHOD FOR IC WIRING YIELD OPTIMIZATION, INCLUDING WIRE WIDENING DURING AND AFTER ROUTING | COHN, JOHN M. |
| 11277663 | Not Issued | 20 | 03/28/2006 | METHOD AND STRUCTURE FOR DEFECT MONITORING OF SEMICONDUCTOR DEVICES USING POWER BUS WIRING GRIDS | COHN, JOHN M. |
| 11280008 | Not Issued | 94 | 11/16/2005 | UTILIZING CLOCK SHIELD AS DEFECT MONITOR | COHN, JOHN M. |
| 11381369 | Not Issued | 20 | 05/03/2006 | PRINTING AND COPYING FAULT MONITORING USING COVER SHEETS | COHN, JOHN M. |
| 08253898 | 5535134 | 150 | 06/03/1994 | OBJECT PLACEMENT AID | COHN, JOHN M. |
| 08549405 | 5745735 | 250 | 10/26/1995 | LOCALIZED SIMULATED ANNEALING | COHN, JOHN M. |
| 08597743 | 5757657 | 150 | 02/07/1996 | ADAPTIVE INCREMENTAL PLACEMENT OF CIRCUITS ON VLSI CHIP | COHN, JOHN M. |
| 09296369 | 6430733 | 150 | 04/22/1999 | CONTEXTUAL BASED GROUNDRULE COMPENSATION METHOD OF MASK DATA SET GENERATION | COHN, JOHN M. |
| 09334980 | Not Issued | 163 | 06/17/1999 | LOCATION BASED CELL PROXIMITY CORRECTION METHOD | COHN, JOHN M. |
| 09475799 | 6751744 | 150 | 12/30/1999 | METHOD OF INTEGRATED CIRCUIT DESIGN CHECKING USING PROGRESSIVE INDIVIDUAL NETWORK ANALYSIS | COHN, JOHN M. |
| 60264215 | Not Issued | 159 | 01/25/2001 | Heart valve implantation device and method | COHN, JOHN M. |
| 09682473 | 7071757 | 150 | 09/06/2001 | CLOCK SIGNAL DISTRIBUTION UTILIZING DIFFERENTIAL SINUSOIDAL SIGNAL PAIR | COHN, JOHN MAXWELL |
| 09683276 | 6651230 | 150 | 12/07/2001 | METHOD FOR REDUCING DESIGN EFFECT OF WEAROUT MECHANISMS ON SIGNAL SKEW IN INTEGRATED CIRCUIT DESIGN | COHN, JOHN MAXWELL |
| 09750884 | 6479974 | 150 | 12/28/2000 | STACKED VOLTAGE RAILS FOR LOW-VOLTAGE DC DISTRIBUTION | COHN, JOHN MAXWELL |
| 09862427 | 6832361 | 150 | 05/21/2001 | SYSTEM AND METHOD FOR | COHN, JOHN MAXWELL |

| | | | | | |
|---|---|---|---|---|---|
| | | | | ANALYZING POWER DISTRIBUTION USING STATIC TIMING ANALYSIS | |
| 09928573 | 6711719 | 150 | 08/13/2001 | METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION IN VLSI CIRCUIT DESIGNS | COHN, JOHN MAXWELL |

Search and Display More Records.

**Search Another: Inventor** **Last Name** COHN **First Name** JOHN Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

PALM INTRANET

Day : Saturday
Date: 6/17/2006
Time: 09:58:38

## Inventor Name Search Result

Your Search was:

Last Name = GOODNOW
First Name = KENNETH

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|---|---|---|---|---|---|
| 09073999 | 6658634 | 150 | 05/07/1998 | LOGIC POWER OPTIMIZATION ALGORITHM | GOODNOW, KENNETH |
| 09103383 | Not Issued | 161 | 06/24/1998 | LOW POWER STAND-BY MODE USING COMPRESSED DATA AND METHOD FOR USING SAME | GOODNOW, KENNETH J |
| 09492624 | Not Issued | 161 | 01/27/2000 | METHOD FOR IP CORE PROTECTION IN ASIC DESIGNS | GOODNOW, KENNETH J. |
| 09682835 | 6541997 | 150 | 10/23/2001 | CLOCKLESS IMPEDANCE CONTROLLER | GOODNOW, KENNETH J. |
| 09709872 | 6604174 | 150 | 11/10/2000 | PERFORMANCE BASED SYSTEM AND METHOD FOR DYNAMIC ALLOCATION OF A UNIFIED MULTIPORT CACHE | GOODNOW, KENNETH J. |
| 09777365 | Not Issued | 161 | 02/05/2001 | Directed least recently used cache replacement method | GOODNOW, KENNETH J. |
| 10064582 | Not Issued | 94 | 07/29/2002 | SYSTEM AND METHOD FOR CORRECTING TIMING SIGNALS IN INTEGRATED CIRCUITS | GOODNOW, KENNETH J. |
| 10248527 | Not Issued | 61 | 01/27/2003 | Dual time sliced circular bus | GOODNOW, KENNETH J. |
| 10249568 | Not Issued | 93 | 04/19/2003 | WIRELESS COMMUNICATION SYSTEM WITHIN A SYSTEM ON A CHIP | GOODNOW, KENNETH J. |
| 10249684 | 6825711 | 150 | 04/30/2003 | POWER REDUCTION BY STAGE IN INTEGRATED CIRCUIT | GOODNOW, KENNETH J. |
| 10604328 | Not Issued | 30 | 07/11/2003 | POWER DOWN PROCESSING ISLANDS | GOODNOW, KENNETH J. |
| 10604410 | Not Issued | 41 | 07/18/2003 | FIBER OPTIC TRANSMISSION LINES ON AN SOC | GOODNOW, KENNETH J. |
| 10605366 | Not Issued | 41 | 09/25/2003 | SEMICONDUCTOR DEVICE COMPRISING A PLURALITY OF MEMORY STRUCTURES | GOODNOW, KENNETH J. |
| 10605603 | 6954085 | 150 | 10/13/2003 | SYSTEM AND METHOD FOR DYNAMICALLY EXECUTING A FUNCTION IN A PROGRAMMABLE LOGIC ARRAY | GOODNOW, KENNETH J. |

| | | | | | |
|---|---|---|---|---|---|
| 10692193 | Not Issued | 30 | 10/23/2003 | Method and structure for replacing faulty operating code contained in a ROM for a processor | GOODNOW, KENNETH J. |
| 10707304 | Not Issued | 30 | 12/04/2003 | MULTIPROCESSOR CODE FIX USING A LOCAL CACHE | GOODNOW, KENNETH J. |
| 10707323 | Not Issued | 41 | 12/05/2003 | METHOD OF SELECTIVELY BUILDING REDUNDANT LOGIC STRUCTURES TO IMPROVE FAULT TOLERANCE | GOODNOW, KENNETH J. |
| 10709809 | Not Issued | 30 | 05/28/2004 | METHOD FOR SYSTEM LEVEL PROTECTION OF FIELD PROGRAMMABLE LOGIC DEVICES | GOODNOW, KENNETH J. |
| 10711082 | Not Issued | 41 | 08/20/2004 | COMMUNICATION SYSTEMS AND METHODS USING MICROELECTRONICS POWER DISTRIBUTION NETWORK | GOODNOW, KENNETH J. |
| 10711084 | Not Issued | 61 | 08/20/2004 | SYSTEM AND METHOD FOR ARBITRATION BETWEEN SHARED PERIPHERAL CORE DEVICES IN SYSTEM ON CHIP ARCHITECTURES | GOODNOW, KENNETH J. |
| 10725712 | 7065733 | 150 | 12/02/2003 | METHOD FOR MODIFYING THE BEHAVIOR OF A STATE MACHINE | GOODNOW, KENNETH J. |
| 10729750 | 6996795 | 150 | 12/04/2003 | DATA PROCESSING IN DIGITAL SYSTEMS | GOODNOW, KENNETH J. |
| 10904259 | Not Issued | 20 | 11/01/2004 | METHOD AND APPARATUS FOR SERVICING THREADS WITHIN A MULTI-PROCESSOR SYSTEM | GOODNOW, KENNETH J. |
| 10906388 | Not Issued | 30 | 02/17/2005 | SYSTEM AND METHOD FOR SYSTEM-ON-CHIP INTERCONNECT VERIFICATION | GOODNOW, KENNETH J. |
| 10906476 | Not Issued | 30 | 02/22/2005 | METHOD OF SWITCHING VOLTAGE ISLANDS IN INTEGRATED CIRCUITS | GOODNOW, KENNETH J. |
| 10908597 | Not Issued | 30 | 05/18/2005 | A METHOD AND APPARATUS FOR TRANSFERRING DATA BETWEEN CORES IN AN INTEGRATED CIRCUIT | GOODNOW, KENNETH J. |
| 11160601 | Not Issued | 20 | 06/30/2005 | METHOD AND APPARATUS FOR MONITORING INTEGRATED CIRCUIT TEMPERATURE THROUGH DETERMINISTIC PATH DELAYS | GOODNOW, KENNETH J. |
| 11160609 | Not Issued | 30 | 06/30/2005 | APPARATUS AND METHOD FOR IMPLEMENTING AN INTEGRATED CIRCUIT IP CORE LIBRARY ARCHITECTURE | GOODNOW, KENNETH J. |
| 11162997 | Not Issued | 30 | 09/30/2005 | FPGA POWERUP TO KNOWN FUNCTIONAL STATE | GOODNOW, KENNETH J. |
| 11164646 | Not | 20 | 11/30/2005 | METHOD AND SYSTEM FOR | GOODNOW, KENNETH J. |

| | | | | | |
|---|---|---|---|---|---|
| | Issued | | | EXTENDING THE USEFUL LIFE OF ANOTHER SYSTEM | |
| 11181053 | Not Issued | 25 | 07/14/2005 | System and method for dynamically executing a function in a programmable logic array | GOODNOW, KENNETH J. |
| 11272884 | Not Issued | 25 | 11/14/2005 | Data processing in digital systems | GOODNOW, KENNETH J. |
| 11275536 | Not Issued | 25 | 01/12/2006 | METHOD FOR INCREASING THE MANUFACTURING YIELD OF PROGRAMMABLE LOGIC DEVICES | GOODNOW, KENNETH J. |
| 11276236 | Not Issued | 25 | 02/20/2006 | PROCESSOR PIPELINE ARCHITECTURE LOGIC STATE RETENTION SYSTEMS AND METHODS | GOODNOW, KENNETH J. |
| 11279507 | Not Issued | 20 | 04/12/2006 | DETERMINING HISTORY STATE OF DATA IN DATA RETAINING DEVICE BASED ON STATE OF PARTIALLY DEPLETED SILICON-ON-INSULATOR | GOODNOW, KENNETH J. |
| 11279639 | Not Issued | 30 | 04/13/2006 | DETERMINING RELATIVE AMOUNT OF USAGE OF DATA RETAINING DEVICE BASED ON POTENTIAL OF CHARGE STORING DEVICE | GOODNOW, KENNETH J. |
| 11279666 | Not Issued | 20 | 04/13/2006 | METHOD OF MANUFACTURING INTEGRATED CIRCUITS USING PRE-MADE AND PRE-QUALIFIED EXPOSURE MASKS FOR SELECTED BLOCKS OF CIRCUITRY | GOODNOW, KENNETH J. |
| 11371833 | Not Issued | 25 | 03/09/2006 | FPGA powerup to known functional state | GOODNOW, KENNETH J. |
| 11380799 | Not Issued | 20 | 04/28/2006 | STRUCTURE AND METHOD FOR IMPLEMENTING OXIDE LEAKAGE BASED VOLTAGE DIVIDER NETWORK FOR INTEGRATED CIRCUIT DEVICES | GOODNOW, KENNETH J. |
| 11410829 | Not Issued | 25 | 04/24/2006 | Wireless communication system within a system on a chip | GOODNOW, KENNETH J. |
| 08504347 | 5710892 | 250 | 07/19/1995 | SYSTEM AND METHOD FOR ASYNCHRONOUS DUAL BUS CONVERSION USING DOUBLE STATE MACHINES | GOODNOW, KENNETH J. |
| 08751465 | 5781922 | 150 | 11/19/1996 | PAGE BOUNDARY CACHES | GOODNOW, KENNETH J. |
| 08751468 | 6026471 | 150 | 11/19/1996 | ANTICIPATING CACHE MEMORY LOADER AND METHOD | GOODNOW, KENNETH J. |
| 08770355 | 6141351 | 150 | 12/20/1996 | RADIO FREQUENCY BUS FOR BROADBAND MICROPROCESSOR COMMUNICATIONS | GOODNOW, KENNETH J. |
| | | | | | |

| | | | | | |
|---|---|---|---|---|---|
| 08835126 | Not Issued | 161 | 04/04/1997 | PREDICTIVE CACHE LOADING BY PROGRAM ADDRESS DISCONTINUITY HISTORY | GOODNOW, KENNETH J. |
| 09054459 | 6134704 | 150 | 04/03/1998 | INTEGRATED CIRCUIT MACRO APPARATUS | GOODNOW, KENNETH J. |
| 09056300 | 6167524 | 150 | 04/06/1998 | APPARATUS AND METHOD FOR EFFICIENT BATTERY UTILIZATION IN PORTABLE PERSONAL COMPUTERS | GOODNOW, KENNETH J. |
| 09074442 | 6081135 | 150 | 05/07/1998 | DEVICE AND METHOD TO REDUCE POWER CONSUMPTION IN INTEGRATED SEMICONDUCTOR DEVICES | GOODNOW, KENNETH J. |
| 09120211 | 6011383 | 150 | 07/21/1998 | LOW POWERING APPARATUS FOR AUTOMATIC REDUCTION OF POWER IN ACTIVE AND STANDBY MODES | GOODNOW, KENNETH J. |
| 09129921 | 6275968 | 150 | 08/06/1998 | APPARATUS AND METHOD TO REDUCE NODE TOGGLING IN SEMICONDUCTOR DEVICES | GOODNOW, KENNETH J. |

Search and Display More Records.

**Search Another: Inventor** **Last Name** GOODNOW **First Name** KENNETH Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

Day : Saturday
Date: 6/17/2006
Time: 10:00:10

PALM INTRANET

## Inventor Name Search Result

Your Search was:

Last Name = STOUT
First Name = DOUGLAS

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|---|---|---|---|---|---|
| 10919116 | Not Issued | 20 | 08/16/2004 | Molded pump | STOUT, DOUGLAS L. |
| 60537537 | Not Issued | 159 | 01/20/2004 | Molded pump | STOUT, DOUGLAS L. |
| 09657081 | 6262873 | 150 | 09/07/2000 | Method for providing ESD protection for an integrated circuit | STOUT, DOUGLAS W. |
| 09666632 | 6292343 | 150 | 09/21/2000 | ASIC book to provide ESD protection on an integrated circuit | STOUT, DOUGLAS W. |
| 09678742 | 6725439 | 150 | 10/04/2000 | METHOD OF AUTOMATED DESIGN AND CHECKING FOR ESD ROBUSTNESS | STOUT, DOUGLAS W. |
| 09777286 | 6362653 | 150 | 02/06/2001 | High voltage tolerant receivers | STOUT, DOUGLAS W. |
| 09895778 | 6545521 | 150 | 06/29/2001 | LOW SKEW, POWER SEQUENCE INDEPENDENT CMOS RECEIVER DEVICE | STOUT, DOUGLAS W. |
| 10063425 | 6667648 | 150 | 04/23/2002 | VOLTAGE ISLAND COMMUNICATIONS CIRCUITS | STOUT, DOUGLAS W. |
| 10064504 | 6577178 | 150 | 07/23/2002 | TRANSIENT GATE TUNNELING CURRENT CONTROL | STOUT, DOUGLAS W. |
| 10065201 | 6820240 | 150 | 09/25/2002 | VOLTAGE ISLAND CHIP IMPLEMENTATION | STOUT, DOUGLAS W. |
| 10065202 | 6779163 | 150 | 09/25/2002 | VOLTAGE ISLAND DESIGN PLANNING | STOUT, DOUGLAS W. |
| 10108687 | 6493257 | 150 | 03/27/2002 | CMOS STATE SAVING LATCH | STOUT, DOUGLAS W. |
| 10248329 | 6891207 | 150 | 01/09/2003 | ELECTROSTATIC DISCHARGE PROTECTION NETWORKS FOR TRIPLE WELL SEMICONDUCTOR DEVICES | STOUT, DOUGLAS W. |
| 10249684 | 6825711 | 150 | 04/30/2003 | POWER REDUCTION BY STAGE IN INTEGRATED CIRCUIT | STOUT, DOUGLAS W. |
| 10604277 | Not Issued | 71 | 07/08/2003 | NESTED VOLTAGE ISLAND ARCHITECTURE | STOUT, DOUGLAS W. |
| 10604328 | Not Issued | 30 | 07/11/2003 | POWER DOWN PROCESSING ISLANDS | STOUT, DOUGLAS W. |

| | | | | | |
|---|---|---|---|---|---|
| 10605483 | Not Issued | 93 | 10/02/2003 | ELECTROSTATIC DISCHARGE PROTECTION NETWORKS FOR TRIPLE WELL SEMICONDUCTOR DEVICES | STOUT, DOUGLAS W. |
| 10605750 | 6927614 | 150 | 10/23/2003 | HIGH PERFORMANCE STATE SAVING CIRCUIT | STOUT, DOUGLAS W. |
| 10711431 | Not Issued | 41 | 09/17/2004 | METHOD AND APPARATUS FOR DEPOPULATING PERIPHERAL INPUT/OUTPUT CELLS | STOUT, DOUGLAS W. |
| 10867914 | 6883152 | 150 | 06/15/2004 | VOLTAGE ISLAND CHIP IMPLEMENTATION | STOUT, DOUGLAS W. |
| 10906476 | Not Issued | 30 | 02/22/2005 | METHOD OF SWITCHING VOLTAGE ISLANDS IN INTEGRATED CIRCUITS | STOUT, DOUGLAS W. |
| 10907499 | Not Issued | 30 | 04/04/2005 | METHOD AND APPARATUS OF OPTIMIZING THE IO COLLAR OF A PERIPHERAL IMAGE | STOUT, DOUGLAS W. |
| 11095327 | Not Issued | 30 | 03/31/2005 | Voltage dependent parameter analysis | STOUT, DOUGLAS W. |
| 11161334 | Not Issued | 93 | 07/29/2005 | SYSTEM AND METHOD FOR POWER GATING | STOUT, DOUGLAS W. |
| 11164040 | Not Issued | 25 | 11/08/2005 | METHOD AND APPARATUS FOR STORING CIRCUIT CALIBRATION INFORMATION | STOUT, DOUGLAS W. |
| 11277385 | Not Issued | 20 | 03/24/2006 | STATIC TIMING SLACKS ANALYSIS AND MODIFICATION | STOUT, DOUGLAS W. |
| 11380799 | Not Issued | 20 | 04/28/2006 | STRUCTURE AND METHOD FOR IMPLEMENTING OXIDE LEAKAGE BASED VOLTAGE DIVIDER NETWORK FOR INTEGRATED CIRCUIT DEVICES | STOUT, DOUGLAS W. |
| 07471249 | 5127008 | 150 | 01/25/1990 | INTEGRATED CIRCUIT DRIVER INHIBIT CONTROL TEST METHOD | STOUT, DOUGLAS W. |
| 07534406 | 5134311 | 150 | 06/07/1990 | SELF-ADJUSTING IMPEDANCE MATCHING DRIVER | STOUT, DOUGLAS W. |
| 07595911 | 5151619 | 150 | 10/11/1990 | CMOS OFF CHIP DRIVER CIRCUIT | STOUT, DOUGLAS W. |
| 07764499 | 5195412 | 150 | 09/20/1991 | NOTCHING AND SHEARING MACHINE FOR EXTERIOR SIDING PANELS AND METHOD OF USING SAME | STOUT, DOUGLAS W. |
| 08431882 | 5644265 | 150 | 05/01/1995 | OFF-CHIP DRIVER FOR MIXED VOLTAGE APPLICATIONS | STOUT, DOUGLAS W. |
| 08595054 | Not Issued | 166 | 01/31/1996 | INTEGRATED CIRCUIT CHIP HAVING GATE ARRAY BOOK PERSONALIZATION USING LOCAL INTERCONNECT | STOUT, DOUGLAS W. |
| 09015819 | Not | 161 | 01/29/1998 | METHOD OF AUTOMATED DESIGN | STOUT, DOUGLAS W. |

| | | | | | |
|---|---|---|---|---|---|
| | Issued | | | AND CHECKING FOR ESD ROBUSTNESS | |
| 09121515 | 6087881 | 150 | 07/23/1998 | INTEGRATED CIRCUIT DUAL LEVEL SHIFT PREDRIVE CIRCUIT | STOUT, DOUGLAS W. |
| 09183707 | 6140846 | 150 | 10/30/1998 | DRIVER CIRCUIT CONFIGURED FOR USE WITH RECEIVER | STOUT, DOUGLAS W. |
| 09224766 | 6157530 | 150 | 01/04/1999 | ESD PROTECTION CIRCUIT FOR MULTIPLE POWER SUUPLY ENVIRONMENTS | STOUT, DOUGLAS W. |
| 09754156 | 6670683 | 150 | 01/04/2001 | COMPOSITE TRANSISTOR HAVING A SLEW-RATE CONTROL | STOUT, DOUGLAS WILLARD |
| 09758054 | 6570401 | 150 | 01/10/2001 | DUAL RAIL POWER SUPPLY SEQUENCE TOLERANT OFF-CHIP DRIVER | STOUT, DOUGLAS WILLARD |
| 10063504 | 6731154 | 150 | 05/01/2002 | GLOBAL VOLTAGE BUFFER FOR VOLTAGE ISLANDS | STOUT, DOUGLAS WILLARD |
| 08812623 | 5867052 | 150 | 03/07/1997 | OFF-CHIP DRIVER FOR MIXED VOLTAGE APPLICATIONS | STOUT, DOUGLAS WILLARD |
| 08871743 | 5969554 | 150 | 06/09/1997 | MULTI-FUNCTION PRE-DRIVER CIRCUIT WITH SLEW WITH SLEW RATE CONTROL, TRI-STATE OPERTION, AND LEVEL SHIFTING | STOUT, DOUGLAS WILLARD |
| 08885494 | Not Issued | 161 | 06/30/1997 | INTERGRATED CIRCUIT CHIP HAVING GATE ARRAY BOOK PERSONALIZATION USING LOCAL INTERCONNECT | STOUT, DOUGLAS WILLARD |

# Inventor Search Completed: No Records to Display.

**Search Another: Inventor** **Last Name** STOUT **First Name** DOUGLAS Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

PALM INTRANET

Day : Saturday
Date: 6/17/2006
Time: 10:02:28

## Inventor Name Search Result

Your Search was:

Last Name = VENTRONE
First Name = SEBASTIAN

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|---|---|---|---|---|---|
| 07796194 | 5357617 | 150 | 11/22/1991 | METHOD AND APPARATUS FOR SUBSTANTIALLY CONCURRENT MULTIPLE INSTRUCTION THREAD PROCESSING BY A SINGLE PIPELINE PROCESSOR | VENTRONE, SEBASTIAN |
| 08927950 | 6405234 | 150 | 09/11/1997 | FULL TIME OPERATING SYSTEM | VENTRONE, SEBASTIAN |
| 09260453 | 6269468 | 150 | 03/02/1999 | SPLIT I/O CIRCUIT FOR PERFORMANCE OPTIMIZATION OF DIGITAL CIRCUITS | VENTRONE, SEBASTIAN |
| 09683778 | Not Issued | 95 | 02/13/2002 | HUB/ROUTER FOR COMMUNICATION BETWEEN CORES USING CARTESIAN COORDINATES | VENTRONE, SEBASTIAN |
| 10248314 | Not Issued | 71 | 01/08/2003 | A Voltage Level Bus Protocol For Transferring Data | VENTRONE, SEBASTIAN R |
| 10604174 | 6954920 | 150 | 06/30/2003 | METHOD, PROGRAM PRODUCT, AND DESIGN TOOL FOR AUTOMATIC TRANSMISSION LINE SELECTION IN APPLICATION SPECIFIC INTEGRATED CIRCUITS | VENTRONE, SEBASTIAN T |
| 09103383 | Not Issued | 161 | 06/24/1998 | LOW POWER STAND-BY MODE USING COMPRESSED DATA AND METHOD FOR USING SAME | VENTRONE, SEBASTIAN T |
| 09615146 | 6636995 | 150 | 07/13/2000 | METHOD OF AUTOMATIC LATCH INSERTION FOR TESTING APPLICATION SPECIFIC INTEGRATED CIRCUITS | VENTRONE, SEBASTIAN T |
| 09492624 | Not Issued | 161 | 01/27/2000 | METHOD FOR IP CORE PROTECTION IN ASIC DESIGNS | VENTRONE, SEBASTIAN T. |
| 09524661 | 6282144 | 150 | 03/13/2000 | Multi-ported memory with asynchronous and synchronous protocol | VENTRONE, SEBASTIAN T. |
| 09602369 | 6978234 | 150 | 06/23/2000 | CONFIGURABLE REAL PROTOTYPE HARDWARE USING CORES AND MEMORY MACROS | VENTRONE, SEBASTIAN T. |
| 09641425 | 6304122 | 150 | 08/17/2000 | Low power LSSD flip flops and a flushable single clock splitter for flip flops | VENTRONE, SEBASTIAN T. |
| 09681077 | 6880074 | 150 | 12/22/2000 | IN-LINE CODE SUPPRESSION | VENTRONE, |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | SEBASTIAN T. |
| 09709872 | 6604174 | 150 | 11/10/2000 | PERFORMANCE BASED SYSTEM AND METHOD FOR DYNAMIC ALLOCATION OF A UNIFIED MULTIPORT CACHE | VENTRONE, SEBASTIAN T. |
| 09713829 | 6792582 | 150 | 11/15/2000 | CONCURRENT LOGICAL AND PHYSICAL CONSTRUCTION OF VOLTAGE ISLANDS FOR MIXED SUPPLY VOLTAGE DESIGNS | VENTRONE, SEBASTIAN T. |
| 09750969 | 6687883 | 150 | 12/28/2000 | SYSTEM AND METHOD FOR INSERTING LEAKAGE REDUCTION CONTROL IN LOGIC CIRCUITS | VENTRONE, SEBASTIAN T. |
| 09781369 | 6985004 | 150 | 02/12/2001 | WIRING OPTIMIZATIONS FOR POWER | VENTRONE, SEBASTIAN T. |
| 09805137 | 6964026 | 150 | 03/14/2001 | A METHOD OF UPDATING A SEMICONDUCTOR DESIGN | VENTRONE, SEBASTIAN T. |
| 09805138 | Not Issued | 161 | 03/14/2001 | Microprocessor including controller for reduced power consumption and method therefor | VENTRONE, SEBASTIAN T. |
| 09805200 | Not Issued | 93 | 03/14/2001 | MICROPROCESSOR INCLUDING CONTROLLER FOR REDUCED POWER CONSUMPTION AND METHOD THEREFOR | VENTRONE, SEBASTIAN T. |
| 09832520 | 6720673 | 150 | 04/11/2001 | VOLTAGE ISLAND FENCING | VENTRONE, SEBASTIAN T. |
| 09852784 | 6535016 | 150 | 05/11/2001 | METHOD AND CIRCUIT FOR PROVIDING COPY PROTECTION IN AN APPLICATION-SPECIFIC INTEGRATED CIRCUIT | VENTRONE, SEBASTIAN T. |
| 09895778 | 6545521 | 150 | 06/29/2001 | LOW SKEW, POWER SEQUENCE INDEPENDENT CMOS RECEIVER DEVICE | VENTRONE, SEBASTIAN T. |
| 09928573 | 6711719 | 150 | 08/13/2001 | METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION IN VLSI CIRCUIT DESIGNS | VENTRONE, SEBASTIAN T. |
| 10001686 | Not Issued | 71 | 10/23/2001 | Pervasive proactive project planner | VENTRONE, SEBASTIAN T. |
| 10064493 | 6794706 | 150 | 07/22/2002 | APPLICATIONS OF SPACE-CHARGE-LIMITED CONDUCTION INDUCED CURRENT INCREASE IN NITRIDE-OXIDE DIELECTRIC CAPACITORS: VOLTAGE REGULATOR FOR POWER SUPPLY SYSTEM AND OTHERS | VENTRONE, SEBASTIAN T. |
| 10064582 | Not Issued | 94 | 07/29/2002 | SYSTEM AND METHOD FOR CORRECTING TIMING SIGNALS IN INTEGRATED CIRCUITS | VENTRONE, SEBASTIAN T. |
| 10249568 | Not Issued | 93 | 04/19/2003 | WIRELESS COMMUNICATION SYSTEM WITHIN A SYSTEM ON A | VENTRONE, SEBASTIAN T. |

| | | | | | |
|---|---|---|---|---|---|
| | | | | CHIP | |
| 10249684 | 6825711 | 150 | 04/30/2003 | POWER REDUCTION BY STAGE IN INTEGRATED CIRCUIT | VENTRONE, SEBASTIAN T. |
| 10604178 | Not Issued | 93 | 06/30/2003 | RANDOM NUMBER GENERATOR | VENTRONE, SEBASTIAN T. |
| 10604205 | 7065602 | 150 | 07/01/2003 | CIRCUIT AND METHOD FOR PIPELINED INSERTION | VENTRONE, SEBASTIAN T. |
| 10604279 | 7058914 | 150 | 07/08/2003 | AUTOMATIC LATCH COMPRESSION/REDUCTION | VENTRONE, SEBASTIAN T. |
| 10604328 | Not Issued | 30 | 07/11/2003 | POWER DOWN PROCESSING ISLANDS | VENTRONE, SEBASTIAN T. |
| 10604410 | Not Issued | 41 | 07/18/2003 | FIBER OPTIC TRANSMISSION LINES ON AN SOC | VENTRONE, SEBASTIAN T. |
| 10605366 | Not Issued | 41 | 09/25/2003 | SEMICONDUCTOR DEVICE COMPRISING A PLURALITY OF MEMORY STRUCTURES | VENTRONE, SEBASTIAN T. |
| 10605591 | Not Issued | 41 | 10/10/2003 | METHOD AND APPARATUS FOR MEMORY ALLOCATION | VENTRONE, SEBASTIAN T. |
| 10605603 | 6954085 | 150 | 10/13/2003 | SYSTEM AND METHOD FOR DYNAMICALLY EXECUTING A FUNCTION IN A PROGRAMMABLE LOGIC ARRAY | VENTRONE, SEBASTIAN T. |
| 10605884 | 6934656 | 150 | 11/04/2003 | AUTO-LINKING OF FUNCTION LOGIC STATE WITH TESTCASE REGRESSION LIST | VENTRONE, SEBASTIAN T. |
| 10680756 | Not Issued | 93 | 10/07/2003 | DATA ACKNOWLEDGMENT USING IMPEDANCE MISMATCHING | VENTRONE, SEBASTIAN T. |
| 10707068 | 7000214 | 150 | 11/19/2003 | METHOD FOR DESIGNING AN INTEGRATED CIRCUIT HAVING MULTIPLE VOLTAGE DOMAINS | VENTRONE, SEBASTIAN T. |
| 10707323 | Not Issued | 41 | 12/05/2003 | METHOD OF SELECTIVELY BUILDING REDUNDANT LOGIC STRUCTURES TO IMPROVE FAULT TOLERANCE | VENTRONE, SEBASTIAN T. |
| 10709754 | Not Issued | 30 | 05/26/2004 | A SYSTEM AND METHOD OF PROVIDING ERROR DETECTION AND CORRECTION CAPABILITY IN AN INTEGRATED CIRCUIT USING REDUNDANT LOGIC CELLS OF AN EMBEDDED FPGA | VENTRONE, SEBASTIAN T. |
| 10710745 | 7053712 | 150 | 07/30/2004 | METHOD AND APPARATUS FOR CONTROLLING COMMON-MODE OUTPUT VOLTAGE IN FULLY DIFFERENTIAL AMPLIFIERS | VENTRONE, SEBASTIAN T. |
| 10725712 | 7065733 | 150 | 12/02/2003 | METHOD FOR MODIFYING THE BEHAVIOR OF A STATE MACHINE | VENTRONE, SEBASTIAN T. |
| 10729750 | 6996795 | 150 | 12/04/2003 | DATA PROCESSING IN DIGITAL SYSTEMS | VENTRONE, SEBASTIAN T. |

| | | | | | |
|---|---|---|---|---|---|
| 10729751 | Not Issued | 41 | 12/04/2003 | Digital reliability monitor having autonomic repair and notification capability | VENTRONE, SEBASTIAN T. |
| 10731296 | Not Issued | 71 | 12/09/2003 | FPGA blocks with adjustable porosity pass thru | VENTRONE, SEBASTIAN T. |
| 10832658 | Not Issued | 30 | 04/27/2004 | Asynchronous packet based dual port link list header and data credit management structure | VENTRONE, SEBASTIAN T. |
| 10863194 | Not Issued | 30 | 06/08/2004 | Digital reliability monitor having autonomic repair and notification capability | VENTRONE, SEBASTIAN T. |
| 10904397 | Not Issued | 30 | 11/08/2004 | METHOD AND APPARATUS FOR CONVERTING GLOBALLY CLOCK-GATED CIRCUITS TO LOCALLY CLOCK-GATED CIRCUITS | VENTRONE, SEBASTIAN T. |

Search and Display More Records.

**Search Another: Inventor** **Last Name** VENTRONE **First Name** SEBASTIAN Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

**Nothing Found**

Your search for **+author:rafael +author:blanco** did not return any results.

You may want to try an Advanced Search for additional options.

Please review the Quick Tips below or for more information see the Search Tips.

## Quick Tips

- Enter your search terms in lower case with a space between the terms.

```
sales offices
```

You can also enter a full question or concept in plain language.

```
Where are the sales offices?
```

- Capitalize proper nouns to search for specific people, places, or products.

```
John Colter, Netscape Navigator
```

- Enclose a phrase in double quotes to search for that exact phrase.

```
"museum of natural history" "museum of modern art"
```

- Narrow your searches by using a + if a search term must appear on a page.

```
museum +art
```

- Exclude pages by using a - if a search term must not appear on a page.

```
museum -Paris
```

Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

```
museum +"natural history" dinosaur -Chicago
```

Terms used **cohn j**

Found **16** of **178,880**

Sort results by: relevance

Display results: expanded form

Save results to a Binder

Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 16 of 16

Relevance scale

1 The A to Z of SoCs

Reinaldo A. Bergamaschi, John Cohn

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

**Publisher:** ACM Press

Full text available: pdf(209.48 KB) Additional Information: full citation, abstract, references, citings, index terms

The exploding complexity of new chips and the ever decreasing time-to-market window are forcing fundamental changes in the way systems are designed. The advent of Systems-on-Chip (SoC) based on pre-designed intellectual-property (IP) cores has become an absolute necessity for embedded systems companies to remain competitive. Designing an SoC, however, is extremely complex, as it encompasses a range of difficult problems in hardware and software design. This paper explains a wide range of SoC iss ...

2 Managing power and performance for System-on-Chip designs using Voltage Islands

David E. Lackey, Paul S. Zuchowski, Thomas R. Bednar, Douglas W. Stout, Scott W. Gould, John M. Cohn

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

**Publisher:** ACM Press

Full text available: pdf(96.51 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper discusses Voltage Islands, a system architecture and chip implementation methodology, that can be used to dramatically reduce active and static power consumption for System-on-Chip (SoC) designs. As technology scales for increased circuit density and performance, the need to reduce power consumption increases in significance as designers strive to utilize the advancing silicon capabilities. The consumer product market further drives the need to minimize chip power consumption.Effectiv ...

3 Supporting systolic and memory communication in iWarp

Shekhar Borkar, Robert Cohn, George Cox, Thomas Gross, H. T. Kung, Monica Lam, Margie Levine, Brian Moore, Wire Moore, Craig Peterson, Jim Susman, Jim Sutton, John Urbanski, Jon Webb

May 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 17th annual international symposium on Computer Architecture ISCA '90**, Volume 18 Issue 3a

**Publisher:** ACM Press

Full text available: pdf(2.09 MB) Additional Information: full citation, abstract, references, citings, index terms

iWarp is a parallel architecture developed jointly by Carnegie Mellon University and Intel Corporation. The iWarp communication system supports two widely used interprocessor communication styles: memory communication and systolic communication. This paper describes the rationale, architecture, and implementation for the iWarp communication system. The sending or receiving processor of a message can perform either memory or systolic communication ...

4 Medical care simulation: A study utilizing dynamic simulation modeling

S. H. Cohn, J. F. Brandejs

January 1973 **Proceedings of the 6th conference on Winter simulation**

**Publisher:** ACM Press

Full text available: pdf(21.24 KB) Additional Information: full citation, abstract, index terms

Development and implementation of a dynamic computer-aided simulation model of the Family Practice Units Network affiliated with the University of Toronto is discussed. The medical network is conceptualized in an industrial dynamics framework, as a system of interacting flows of patients, medical staff, capital assets, information, and money. Given a patient demand for medical care, the model will process patient's allocation, hire staff, accumulate capital assets and generate ex ...

5 Nanometer design: place your bets: Nanometer design: place your bets

Andrew B. Kahng, Shekhar Borkar, John Cohn, Antun Domic, Patrick Groeneveld, Louis Scheffer, Jean-Pierre Schoellkopf

June 2003 **Proceedings of the 40th conference on Design automation**

**Publisher:** ACM Press

Full text available: pdf(373.87 KB) Additional Information: full citation

6 WBIA'05: Persistence in dynamic code transformation systems

Vijay Janapa Reddi, Dan Connors, Robert S. Cohn

December 2005 **ACM SIGARCH Computer Architecture News**, Volume 33 Issue 5

**Publisher:** ACM Press

Full text available: pdf(295.49 KB) Additional Information: full citation, abstract, references

Dynamic code transformation systems (DCTS) can broadly be grouped into three distinct categories: optimization, translation and instrumentation. All of these face the critical challenge of minimizing the overhead incurred during transformation since their execution is interleaved with the execution of the application itself. The common DCTS tasks incurring overhead are the identification of frequently executed code sequences, costly analysis of program information, and run-time creation (writing ...

7 Brave new topics 2: affective multimodal human-computer interaction: Affective multimodal human-computer interaction

Maja Pantic, Nicu Sebe, Jeffrey F. Cohn, Thomas Huang

November 2005 **Proceedings of the 13th annual ACM international conference on Multimedia MULTIMEDIA '05**

**Publisher:** ACM Press

Full text available: pdf(252.57 KB) Additional Information: full citation, abstract, references, index terms

Social and emotional intelligence are aspects of human intelligence that have been argued to be better predictors than IQ for measuring aspects of success in life, especially in social interactions, learning, and adapting to what is important. When it comes to machines, not all of them will need such skills. Yet to have machines like computers, broadcast systems, and cars, capable of adapting to their users and of anticipating their wishes, endowing them with the ability to recognize user's affe ...

**Keywords:** affective computing, multimodal human-computer interaction

8 Oral I: Person identification using automatic integration of speech, lip, and face experts

Niall A. Fox, Ralph Gross, Philip de Chazal, Jeffery F. Cohn, Richard B. Reilly

November 2003 **Proceedings of the 2003 ACM SIGMM workshop on Biometrics methods and applications**

**Publisher:** ACM Press

Full text available: pdf(293.18 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a multi-expert person identification system based on the integration of three separate systems employing audio features, static face images and lip motion features respectively. Audio person identification was carried out using a text dependent Hidden Markov Model methodology. Modeling of the lip motion was carried out using Gaussian probability density functions. The static image based identification was carried out using the FaceIt system. Experiments were conducted with 25 ...

**Keywords:** audio, automatic weighting, face, late integration, lips, multi-expert, person identification

9 XML and genomic data

Judith D. Cohn

December 2000 **ACM SIGBIO Newsletter**, Volume 20 Issue 3

**Publisher:** ACM Press

Full text available: pdf(256.02 KB) Additional Information: full citation, abstract, index terms

XML is an extensible, universal format for structured data exchange and documents on the Web. This brief overview highlights examples of current work and future directions for domain-specific XML within the genomic community.

10 Layout tools for analog ICs and mixed-signal SoCs: a survey

Rob A. Rutenbar, John M. Cohn

May 2000 **Proceedings of the 2000 international symposium on Physical design**

**Publisher:** ACM Press

Full text available: pdf(247.03 KB) Additional Information: full citation, references

11 Bimodal expression of emotion by face and voice

Jeffrey F. Cohn, Gary S. Katz

September 1998 **Proceedings of the sixth ACM international conference on Multimedia: Face/gesture recognition and their applications**

**Publisher:** ACM Press

Full text available: pdf(431.60 KB) Additional Information: full citation, references, index terms

12 Pin: building customized program analysis tools with dynamic instrumentation

Chi-Keung Luk, Robert Cohn, Robert Muth, Harish Patil, Artur Klauser, Geoff Lowney, Steven Wallace, Vijay Janapa Reddi, Kim Hazelwood

June 2005 **ACM SIGPLAN Notices , Proceedings of the 2005 ACM SIGPLAN conference on Programming language design and implementation PLDI '05**, Volume 40 Issue 6

**Publisher:** ACM Press

Full text available: pdf(300.61 KB) Additional Information: full citation, abstract, references, citings, index terms

Robust and powerful software instrumentation tools are essential for program analysis tasks such as profiling, performance evaluation, and bug detection. To meet this need, we have developed a new instrumentation system called *Pin*. Our goals are to provide *easy-to-use, portable, transparent*, and *efficient* instrumentation. Instrumentation tools (called *Pintools*) are written in C/C++ using Pin's rich API. Pin follows the model of ATOM,

allowing the tool writer to analyz ...

**Keywords:** dynamic compilation, instrumentation, program analysis tools

**13** Code layout optimizations for transaction processing workloads

Alex Ramirez, Luiz André Barroso, Kourosh Gharachorloo, Robert Cohn, Josep Larriba-Pey, P. Geoffrey Lowney, Mateo Valero

May 2001 **ACM SIGARCH Computer Architecture News , Proceedings of the 28th annual international symposium on Computer architecture ISCA '01**, Volume 29 Issue 2

**Publisher:** ACM Press

Full text available: pdf(746.54 KB) Additional Information: full citation, abstract, references, citings, index terms

Commercial applications such as databases and Web servers constitute the most important market segment for high-performance servers. Among these applications, on-line transaction processing (OLTP) workloads provide a challenging set of requirements for system designs since they often exhibit inefficient executions dominated by a large memory stall component. This behavior arises from large instruction and data footprints and high communication miss rates. A number of recent studies have chara ...

**14** ASIC design in nanometer era - dead or alive?: Pushing ASIC performance in a power envelope

Ruchir Puri, Leon Stok, John Cohn, David Kung, David Pan, Dennis Sylvester, Ashish Srivastava, Sarvesh Kulkarni

June 2003 **Proceedings of the 40th conference on Design automation**

**Publisher:** ACM Press

Full text available: pdf(487.74 KB) Additional Information: full citation, abstract, references, citings, index terms

Power dissipation is becoming the most challenging design constraint in nanometer technologies. Among various design implementation schemes, standard cell ASICs offer the best power efficiency for high-performance applications. The flexibility of ASICs allow for the use of multiple voltages and multiple thresholds to match the performance of critical regions to their timing constraints, and minimize the power everywhere else. We explore the trade-off between multiple supply voltages and multiple ...

**Keywords:** ASIC, design optimization, high-performance, low-power

**15** Session 3: From the Trenches (invited): There is life left in ASICs

Leon Stok, John Cohn

April 2003 **Proceedings of the 2003 international symposium on Physical design**

**Publisher:** ACM Press

Full text available: pdf(71.49 KB) Additional Information: full citation, references, citings, index terms

**Keywords:** ASIC, design cost, design tools

**16** Is nanometer design under control? (panel session)

Andrew B. Kahng, Nancy Nettleton, John Cohn, Shekhar Borkar, Louis Scheffer, Ed Cheng, Sang Wang

June 2001 **Proceedings of the 38th conference on Design automation**

**Publisher:** ACM Press

Full text available: pdf(105.77 KB) Additional Information: full citation, abstract, index terms

As fabrication technology moves to 100 nm and below, profound nanometer effects become critical in developing silicon chips with hundreds of millions of transistors. Both

EDA suppliers and system houses have been re- tooling, and new methodologies have been emerging. Will these efforts meet the challenges of nanometer silicon such as performance closure, power, reliability, manufacturability, and cost? Which aspects of nanometer design are, or are not, under control? This session will consi ...

Results 1 - 16 of 16

**Nothing Found**

Your search for **+author:goodnow +author:k** did not return any results.

You may want to try an Advanced Search for additional options.

Please review the Quick Tips below or for more information see the Search Tips.

## Quick Tips

- Enter your search terms in lower case with a space between the terms.

```
sales offices
```

  You can also enter a full question or concept in plain language.

```
Where are the sales offices?
```

- Capitalize proper nouns to search for specific people, places, or products.

```
John Colter, Netscape Navigator
```

- Enclose a phrase in double quotes to search for that exact phrase.

```
"museum of natural history" "museum of modern art"
```

- Narrow your searches by using a + if a search term must appear on a page.

```
museum +art
```

- Exclude pages by using a - if a search term must not appear on a page.

```
museum -Paris
```

Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

```
museum +"natural history" dinosaur -Chicago
```

Terms used **stout d**

Found **8** of **178,880**

Sort results by relevance

Display results expanded form

Save results to a Binder

Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 8 of 8

Relevance scale

**1** Managing power and performance for System-on-Chip designs using Voltage Islands

David E. Lackey, Paul S. Zuchowski, Thomas R. Bednar, Douglas W. Stout, Scott W. Gould, John M. Cohn

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

**Publisher:** ACM Press

Full text available: pdf(96.51 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper discusses Voltage Islands, a system architecture and chip implementation methodology, that can be used to dramatically reduce active and static power consumption for System-on-Chip (SoC) designs. As technology scales for increased circuit density and performance, the need to reduce power consumption increases in significance as designers strive to utilize the advancing silicon capabilities. The consumer product market further drives the need to minimize chip power consumption.Effectiv ...

**2** Adaptive blocks: a high performance data structure

Quentin F. Stout, Darren L. De Zeeuw, Tamas I. Gombosi, Clinton P. T. Groth, Hal G. Marshall, Kenneth G. Powell

November 1997 **Proceedings of the 1997 ACM/IEEE conference on Supercomputing (CDROM)**

**Publisher:** ACM Press

Full text available: pdf(236.62 KB) Additional Information: full citation, abstract, references, citings

We examine a data structure which uses flexible "adaptivity" to obtain high performance for both serial and parallel computers. The data structure is an adaptive grid which partitions a given region into regular cells. Its closest relatives are cell-based tree decompositions, but there are several important differences which lead to significant performance advantages. Using this block data structure to support adaptive mesh refinement (AMR), we were able to sustain 17 GFLOPS in ideal magnetohydr ...

**Keywords**: adaptive blocks, adaptive mesh refinement (AMR), dynamic data structure, high performance computing, magnetohydrodynamics (MHD), octree, parallel computing, quadtree, spatial decomposition

**3** Adaptive parallel computation of a grand-challenge problem: prediction of the path of a solar-corona mass ejection

Quentin F. Stout, Darren L. De Zeeuw, Tamas I. Gombosi, Clinton P. T. Groth, Hal G. Marshall, Kenneth G. Powell

November 1998 **Proceedings of the 1998 ACM/IEEE conference on Supercomputing (CDROM)**

**Publisher:** IEEE Computer Society
Full text available: html(28.70 KB) Additional Information: full citation, abstract, references

One of the ways that the Sun interacts with the Earth is through the solar wind, which is an ionized multi-component fluid that emanates from the Sun and travels radially outward at hundreds of kilometers per second. Solar-wind transients, such as Coronal Mass Ejections (CME's), can be particularly important. In rare cases, CME's have affected the lower atmosphere of the Earth, causing regional power-grid failures. More regularly, CME's pose threats to satellites and spacecraft. Due to the extre ...

**Keywords**: Riemann solver, adaptive blocks, adaptive mesh refinement (AMR), coronal mass ejection (CME), heliospheric plasma, hyperbolic PDEs, magneto-hydrodynamics (MHD), space weather prediction, upwind methods

4 Session: Diffusive parallelism: a parallel programming model for large scale distributed computation systems

Peter D. Stout, Brian N. Bershad

September 1992 **Proceedings of the 5th workshop on ACM SIGOPS European workshop: Models and paradigms for distributed systems structuring**
**Publisher:** ACM Press
Full text available: pdf(575.62 KB) Additional Information: full citation, abstract, references

The spread of networks and powerful workstations has created an attractive source of parallel computing power. We are exploring a new parallel programming model, called *diffusive parallelism*, designed specifically for use with large scale, distributed computation systems. The model provides a simple, yet powerful, abstraction to the programmer, while making it possible to build a secure, robust, distributed computation system in the presence of long delays, failure, and untrusted user pro ...

5 Optimal parallel construction of Hamiltonian cycles and spanning trees in random graphs

Philip D. MacKenzie, Quentin F. Stout

August 1993 **Proceedings of the fifth annual ACM symposium on Parallel algorithms and architectures**
**Publisher:** ACM Press
Full text available: pdf(702.15 KB) Additional Information: full citation, references, index terms

6 Ultra-fast expected time parallel algorithms

Philip D. MacKenzie, Quentin F. Stout

March 1991 **Proceedings of the second annual ACM-SIAM symposium on Discrete algorithms**
**Publisher:** Society for Industrial and Applied Mathematics
Full text available: pdf(1.07 MB) Additional Information: full citation, references, citings, index terms

7 Introducing parallel algorithms in undergraduate computer science courses (tutorial session)

Bruce R. Maxim, Gregory Bachelis, David James, Quentin Stout

February 1990 **ACM SIGCSE Bulletin , Proceedings of the twenty-first SIGCSE technical symposium on Computer science education SIGCSE '90**, Volume 22 Issue 1
**Publisher:** ACM Press
Full text available: pdf(78.80 KB) Additional Information: full citation, index terms

8 Simulating schedule reovery strategies in manufacturing assembly operations

Patrick J. Starr, Douglas S. Skrien, Robert M. Meyer
December 1986 **Proceedings of the 18th conference on Winter simulation**
**Publisher:** ACM Press

Full text available: pdf(542.30 KB) Additional Information: full citation, abstract, references, citings, index terms

An animated simulation is used to evaluate two workforce management options in response to work stoppages in an electronic assembly workcell. An industrial based workcell consisting of 15 workstations is modeled in the SIMPLE_1 environment. A work stoppage is introduced at a station and the throughput time for each assembly is recorded. Two strategies are compared: one has five worker groups, each serving a set of stations, and the other allows workers to move between groups. Steady state p ...

Results 1 - 8 of 8

Terms used **power** or **voltage island** Found **1** of **178,880**

Sort results by relevance

Display results expanded form

Save results to a Binder

Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 1 of 1

Relevance scale

1 An Iterative Algorithm for Battery-Aware Task Scheduling on Portable Computing Platforms

Jawad Khan, Ranga Vemuri

March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '05**

**Publisher:** IEEE Computer Society

Full text available: pdf(161.55 KB) Additional Information: full citation, abstract, citings, index terms

In this work we consider battery powered portable systems which either have Field Programmable Gate Arrays (FPGA) or voltage and frequency scalable processors as their main processing element. An application is modeled in the form of a precedence task graph at a coarse level of granularity. We assume that for each task in the task graph several unique design-points are available which correspond to different hardware implementations for FPGAs and different voltage-frequency combinations for proc ...

Results 1 - 1 of 1

**No Authors found beginning with letter: rafael blanco**

**OPTION 1**
Quick Find an Author:
Enter a name to locate articles written by that author.

rafael blanco

Example: Enter Lockett S to obtain a list of authors with the last name Lockett and the first initial S.

**OPTION 2**
Browse alphabetically

Select a letter from the list.

A B C D E F G H I J K L M N O P Q R S T U V W X Y Z

OPTION 1
Quick Find an Author:
Enter a name to locate articles written by that author.

cohn john >>

Example: Enter Lockett S to obtain a list of authors with the last name Lockett and the first initial S.

OPTION 2
Browse alphabetically

Select a letter from the list.

A B C D E F G H I J K L M N O P Q R S T U V W X Y Z

**No Authors found beginning with letter: cohn john**

Results for **"(cohn j. m.<in>au)"**
Your search matched **4** of **1356463** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» Search Options

View Session History

New Search

Modify Search

(cohn j. m.<in>au) Search

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

view selected items Select All Deselect All

1. **KOAN/ANAGRAM II: new tools for device-level analog placement and routing**
Cohn, J.M.; Garrod, D.J.; Rutenbar, R.A.; Carley, L.R.;
Solid-State Circuits, IEEE Journal of
Volume 26, Issue 3, Mar 1991 Page(s):330 - 342
Digital Object Identifier 10.1109/4.75012
AbstractPlus | Full Text: PDF(1628 KB) IEEE JNL
Rights and Permissions

2. **Managing power and performance for system-on-chip designs using Voltage Islands**
Lackey, D.E.; Zuchowski, P.S.; Bednar, T.R.; Stout, D.W.; Gould, S.W.; Cohn, J.M.;
Computer Aided Design, 2002. ICCAD 2002. IEEE/ACM International Conference on
10-14 Nov. 2002 Page(s):195 - 202
Digital Object Identifier 10.1109/ICCAD.2002.1167534
AbstractPlus | Full Text: PDF(629 KB) IEEE CNF
Rights and Permissions

3. **New algorithms for placement and routing of custom analog cells in ACACIA**
Cohn, J.M.; Garrod, D.J.; Rutenbar, R.A.; Carley, L.R.;
Custom Integrated Circuits Conference, 1990., Proceedings of the IEEE 1990
13-16 May 1990 Page(s):27.6/1 - 27.6/5
Digital Object Identifier 10.1109/CICC.1990.124815
AbstractPlus | Full Text: PDF(616 KB) IEEE CNF
Rights and Permissions

4. **Techniques for simultaneous placement and routing of custom analog cells in KOAN/ANAGRAM II**
Cohn, J.M.; Garrod, D.J.; Rutenbar, R.A.; Carley, L.R.;
Computer-Aided Design, 1991. ICCAD-91. Digest of Technical Papers., 1991 IEEE International Conference on
11-14 Nov. 1991 Page(s):394 - 397
Digital Object Identifier 10.1109/ICCAD.1991.185285
AbstractPlus | Full Text: PDF(404 KB) IEEE CNF
Rights and Permissions

Results for **"(goodnow k.<in>au)"**
Your search matched **1** of **1356463** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» Search Options

View Session History

New Search

Modify Search

(goodnow k.<in>au) Search

Check to search only within this results set

» Key

Display Format: Citation Citation & Abstract

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

view selected items Select All Deselect All

1. **Standards-compliant IP-based ASIC and SoC design**
Hekmatpour, A.; Goodnow, K.; Hemen Shah;
SOC Conference, 2005. Proceedings. IEEE International
25-28 Sept. 2005 Page(s):322 - 323
Digital Object Identifier 10.1109/SOCC.2005.1554521

AbstractPlus | Full Text: PDF(384 KB) IEEE CNF
Rights and Permissions





Indexed by Inspec

**OPTION 1**
Quick Find an Author:
Enter a name to locate articles written by that author.

stout douglas >>

Example: Enter Lockett S to obtain a list of authors with the last name Lockett and the first initial S.

**OPTION 2**
Browse alphabetically

Select a letter from the list.

A B C D E F G H I J K L M N O P Q R S T U V W X Y Z

**No Authors found beginning with letter: stout douglas**

Results for **"(stout d. w.<in>au)"**
Your search matched **5** of **1356463** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» Search Options

View Session History

New Search

Modify Search

(stout d. w.<in>au) Search >

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

view selected items Select All Deselect All

1. **A SiGe transmitter chipset for CATV video-on-demand systems**
   Ashby, K.B.; Greene, R.E.; Nise, B.E.; Womac, M.D.; Stout, D.W.; Taddiken, A.H.;
   Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International
   2003 Page(s):440 - 506 vol.1
   Digital Object Identifier 10.1109/ISSCC.2003.1234375
   AbstractPlus | Full Text: PDF(47891 KB) | Multimedia IEEE CNF
   Rights and Permissions

2. **Managing power and performance for system-on-chip designs using Voltage Islands**
   Lackey, D.E.; Zuchowski, P.S.; Bednar, T.R.; Stout, D.W.; Gould, S.W.; Cohn, J.M.;
   Computer Aided Design, 2002. ICCAD 2002. IEEE/ACM International Conference on
   10-14 Nov. 2002 Page(s):195 - 202
   Digital Object Identifier 10.1109/ICCAD.2002.1167534
   AbstractPlus | Full Text: PDF(629 KB) IEEE CNF
   Rights and Permissions

3. **The first copper ASICs: A 12M-gate technology**
   Panner, J.H.; Bednar, T.R.; Buffet, P.H.; Kemerer, D.W.; Stout, D.W.; Zuchowski, P.S.;
   Custom Integrated Circuits, 1999. Proceedings of the IEEE 1999
   16-19 May 1999 Page(s):347 - 350
   Digital Object Identifier 10.1109/CICC.1999.777304
   AbstractPlus | Full Text: PDF(472 KB) IEEE CNF
   Rights and Permissions

4. **I/O impedance matching algorithm for high-performance ASICs**
   Zuchowski, P.S.; Panner, J.H.; Stout, D.W.; Adams, J.M.; Chan, F.; Dunn, P.E.; Huber, A.D.; Oler, J.J.;
   ASIC Conference and Exhibit, 1997. Proceedings., Tenth Annual IEEE International
   7-10 Sept. 1997 Page(s):270 - 273
   Digital Object Identifier 10.1109/ASIC.1997.617019
   AbstractPlus | Full Text: PDF(388 KB) IEEE CNF
   Rights and Permissions

5. **VLSI performance compensation for off-chip drivers and clock generation**
   Cox, D.T.; Guertin, D.L.; Johnson, C.L.; Rudolph, B.G.; Williams, R.R.; Piro, R.A.; Stout, D.W.;
   Custom Integrated Circuits Conference, 1989., Proceedings of the IEEE 1989
   15-18 May 1989 Page(s):14.3/1 - 14.3/4
   Digital Object Identifier 10.1109/CICC.1989.56752
   AbstractPlus | Full Text: PDF(248 KB) IEEE CNF
   Rights and Permissions